Dual Edge Count Programmable Frequency Divider

Field of the Invention

5   The present invention relates to frequency dividers.

Background of the Invention

Programmable frequency dividers are utilized in a number of electronic applications. To
10   simplify the following discussion, the present invention will be explained in terms of a phase-
locked loop (PLL) that utilizes such a divider. For example, microwave synthesizers are
commonly used in test equipment to provide a test signal that sweeps a frequency range specified
by the user. A microwave synthesizer can be designed using several approaches, depending on
the performance requirements. The lowest cost approach utilizes a single phase-lock loop (PLL)
15   design. In a single loop design, the output of the synthesizer is divided by a divider and
compared against a reference frequency. Denote the division factor by F_{div}. When the loop is
locked, the output frequency of the synthesizer is F_{div} times the reference frequency.

A conventional programmable divider is constructed from a counter having a register
20   constructed from a number of flip-flops and a comparator that determines when the counter
reaches a predetermined state. For example, the counter can subtract one from the contents of
the register on each clock pulse. The counter is initially loaded with F_{div}. When the counter
reaches zero, the counter outputs a signal and reloads the register with F_{div}. The counter is
decremented, for example, on the leading edge of the input signal.
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In a conventional programmable divider, the input frequency f_{in} is used to trigger all the
flip-flops inside the divider. Hence, all the flip-flops have to operate at f_{in}. Hence, the frequency
response of the counter flip-flops sets the upper limit on the maximum frequency at which the
frequency divider can operate. As the frequency demands placed on microwave PLLs increase,
30   the cost of providing higher frequency dividers becomes significant.

Summary of the Invention

5   The present invention includes a frequency divider having an input frequency divider, an edge counter, and an output generator. The input frequency divider generates an intermediate signal having a frequency of f_i from an input signal having a frequency f_{in}, wherein $f_{in}=Rf_I$, and R is an integer >1. The edge counter generates a value equal to the number of edges in the intermediate signal that have occurred since a reset signal was generated. The output generator

10   generates an output signal when the edge counter value reaches a value Q and generates the reset signal. In one embodiment, the edge counter includes a positive edge counter that generates a positive count value equal to the number of positive going transitions in the intermediate signal since the reset signal, a negative edge counter that generates a negative count value equal to the number of negative going transitions in the intermediate signal since the reset signal, and an

15   adder that generates the sum of the positive count and the negative count.

Brief Description of the Drawings

        Figure 1 is a block diagram of a prior art frequency synthesizer.

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        Figure 2 is a block diagram of a frequency divider according to one embodiment of the present invention.

        Figure 3 illustrates the signals at various locations in the frequency divider shown in

25   Figure 2.

        Figure 4 is a block diagram of a frequency divider according to another embodiment of the present invention.

Figure 5 illustrates the signals at various locations in the frequency divider shown in Figure 4.

Detailed Description of the Preferred Embodiments of the Invention

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The present invention can be more easily understood with reference to Figure 1, which is a block diagram of a prior art frequency synthesizer 10. Synthesizer 10 utilizes a YTO (Yttrium-Iron-Garnat Tuned Oscillator). A YTO is preferred because it provides a high quality microwave oscillator with a wide tuning range and excellent tuning linearity. YTO 17 is controlled by the

10   output of integrator 18 to set the final output frequency F_{out}. The output frequency is divided by a factor of N by divider 14 to generate the signal that is compared with the reference signal F_{ref} in phase detector 13. The reference signal is typically at a fixed frequency F_{ref} generated by dividing the output of a high frequency reference signal generator 11 using a second divider 12.

15   Refer now to Figures 2 and 3. Figure 2 is a block diagram of a frequency divider 100 according to one embodiment of the present invention. Frequency divider 100 utilizes a divide by two circuit 102 to generate a signal having a frequency f_i from the input signal f_{in}. Signal f_i is a square wave. Signal f_i is input to each of two counters 103 and 104, respectively. Counter 103 counts the negative edges in f_i, and counter 104 counts the positive edges in f_i. The sum of the

20   contents of counters 103 and 104 is formed by adder 105, which stores its output in a register in an output generator 106. When the count in this register is equal to Q, output generator 106 generates a signal that is synchronized to the input signal. Hence, the output of output generator 106 has frequency f_{out}, where $f_{out}=f_{in}/Q$. When output generator 106 generates the output signal, output generator 106 resets counters 103 and 104. The various signals and counter values are

25   shown in Figure 3. It should be noted that the present invention requires that the divide factor, Q, be greater than 1.

By using an edge count programmable frequency divider as shown in Figure 2, the input frequency is divided by a factor of 2 first to generate the signal that is actually used by the

30   counters. Hence, there are only 2 or 3 flip-flops that need to be triggered at the high input

frequency, f_{in}, namely the two flip flops in the divide by two counter and the output flip flop of this counter. The other flip-flops are only required to operate at $f_{in}/2$. Hence, the present invention requires many fewer high-speed flip-flops.

5   The above-described embodiments have been explained in terms of a frequency divider. However, an edge-count divider according to the present invention can also be applied on other counters. The present invention divides a counter into two edge counters that operate at half the frequency of the input signal. One counter counts the positive edges and the other counter counts the negative edges. The counts in the two edge counters are then added to provide the final

10   count. Only the divide by two circuit needs to operate at the input frequency; hence, the number of high-frequency flip flops is substantially reduced.

       In principle, the embodiment shown in Figure2 can be generalized to provide a fractional divide circuit. Refer now to Figures 4 and 5, which illustrate a block diagram of an embodiment

15   of the present invention that provides fractional division. To simplify the following discussion, those elements of frequency divider 200 that serve the same function as elements discussed above with reference to Figure 2 have been given the same numeric designations and will not be discussed further here. In this more general embodiment, the divide by 2 shown in Figure 2 at 102 is replaced by a divide by R circuit 202 where R is an integer. The total divide factor is

20   given by (QR)/2, and the output frequency is given by $f_{out}=2f_{in}/(QR)$. For example, consider the case in which R=3 and Q=5, the divide factor would be 7.5 in this case. The various signals and counter values for this case are shown in Figure 5.

       The higher divide factor further reduces the frequency demands on the edge counters.

25   However, the higher divide factor increases the cost of the divide circuit that converts f_{in} to f_i. If R is small, a net saving is still realized.

       Various modifications to the present invention will become apparent to those skilled in the art from the foregoing description and accompanying drawings. Accordingly, the present

30   invention is to be limited solely by the scope of the following claims.